WHAT IS CLAIMED IS:

1. A processor comprising:

a trace generator configured to generate a plurality of traces each including one or more operations, wherein said one or more operations are decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address;

a trace cache memory coupled to said trace generator, wherein said trace cache memory includes a plurality of entries each configured to store one of said plurality of traces;

wherein said trace generator is further configured to restrict each of said plurality of traces to include only operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses.

2. The processor as recited in claim 1, wherein a starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a given one of said one or more operations within each of said plurality of traces.

3. The processor as recited in claim 1, wherein starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a first operation of said one or more operations within each of said plurality of traces.

4. The processor as recited in claim 2, wherein each of said one or more predetermined ranges of contiguous addresses is separated by a predetermined number of contiguous addresses.

5. The processor as recited in claim 2, wherein said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as

determined by said respective address of a given one of said one or more operations and a next N sequential ranges of contiguous addresses, where N is any number.

6. The processor as recited in claim 2, wherein said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next sequential range of contiguous addresses.

7. The processor as recited in claim 1 further comprising a trace cache control unit coupled to said trace cache memory and configured to receive a trace cache probe and to store in a trace cache probe storage, an address corresponding to said trace cache probe until said trace cache probe completes.

8. The processor as recited in claim 7, wherein said trace cache control unit is further configured to determine whether a trace cache probe to a particular address is outstanding in response to receiving a trace cache fetch to said particular address by comparing said particular address to said address corresponding to said trace cache probe stored within said trace cache probe storage.

9. The processor as recited in claim 8, wherein said trace cache control unit is further configured to block said trace cache fetch in response to determining that said trace cache probe to a particular address is outstanding.

10. A method comprising:

generating a trace including one or more operations decoded from one or more instructions, wherein each of said one or more operations is associated with a respective address;

storing said trace in a trace cache entry within a trace cache memory;

restricting said trace to include only operations having respective addresses that fall within one or more predetermined ranges of contiguous addresses.

11. The method as recited in claim 10, wherein a starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a given one of said one or more operations within said trace.

12. The method as recited in claim 10, wherein starting address of said one or more predetermined ranges of contiguous addresses is based upon said respective address of a first operation of said one or more operations within said trace.

13. The method as recited in claim 11, wherein each of said one or more predetermined ranges of contiguous addresses is separated by a predetermined number of contiguous addresses.

14. The method as recited in claim 11, wherein said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next N sequential ranges of contiguous addresses, where N is any number.

15. The method as recited in claim 11, wherein said one or more predetermined ranges of contiguous addresses includes a first range of contiguous addresses as determined by said respective address of a given one of said one or more operations and a next sequential range of contiguous addresses.

16. The method as recited in claim 10 further comprising receiving a trace cache probe and storing in a trace cache probe storage, an address corresponding to said trace cache probe until said trace cache probe completes.

17. The method as recited in claim 16 further comprising in response to receiving a trace cache fetch to a particular address, determining whether a trace cache probe to said

particular address is outstanding by comparing said particular address to said address corresponding to said trace cache probe stored within said trace cache probe storage.

18. The method as recited in claim 17 further comprising blocking said trace cache fetch in response to determining that said trace cache probe to a particular address is outstanding.